REMARKS

I. Introduction

Applicants would like to thank Examiner Phan for the indication of allowable subject matter recited by claims 5 and 7. In response to the Office Action dated December 7, 2004, Applicants have canceled claims 1, 9 and 10, without prejudice or disclaimer, and have rewritten claim 2 into independent format incorporating all claim limitations recited by canceled claim 1. Also, the claim dependency of claims 3, 4 and 6 has been amended to depend on amended claim 2. Additionally Applicants has amended claim 8 so as to further clarify the claimed invention. New claims 11-17 are added. Support for these amendments can be found, for example, in Figs. 1 and 13, and their corresponding sections of the specification. No new matter has been added.

Furthermore, Applicants note that an IDS was filed on January 4, 2005, after the issuance of the pending Office Action. Accordingly, it is respectfully requested that the foregoing document be expressly considered during the prosecution of this application, and that the document be made of record therein. Applicants respectfully request that the PTO-1449 form submitted with the IDS be initialed and returned to the Applicants so as to confirm the IDS was considered.

For the reasons set forth below, Applicants respectfully submit that all pending claims are patentable over the cited prior art references.

II. The Rejection Of Claims 1-4, 6 and 8-10 Under 35 U.S.C. § 103

Claims 1-4, 6 and 8-10 are rejected under 35 U.S.C. § 103(a) as being unpatentable over US Pub No. 2003/0179719 to Kobayashi in view of USP No. 6,408,012 to Sato. In response,

claims 1, 9 and 10 have been canceled, rendering the rejection thereto moot. For the remaining claims, Applicants respectfully traverse the rejection for at least the following reasons.

It is respectfully submitted that Kobayashi and Sato, alone or in combination, do not disclose or suggest the claimed invention. In the pending Office Action, The Examiner relies on Kobayashi for allegedly disclosing a transmission/reception circuit 301 for packetizing the information data supplied from the signal processing circuit 106, a timer circuit 305 for measuring time coinciding with other devices, and a control circuit 306 for controlling the functions of the digital interface 105. The Examiner admits that Kobayashi does not disclose a link core circuit for receiving a packet externally delivered through a bus and sending out the packet...supplied from the packet processing controller by way of a bus, but relies on the link core 101 of Sato to meet to the claimed invention.

However, in doing so, it would appear that the pending rejection merely ***assumes*** that the alleged packet processing controller of Kobayashi is ***capable*** of receiving and processing a packet from the link core 101 of Sato without providing or identifying any support for the allegation. Moreover, the rejection uses that unfounded allegation to further support the allegation that the alleged packet processing controller of Kobayashi ***necessarily*** generates and supplies a packet to be transmitted ***in response*** to the received packet ***back*** to the link core 101 of Sato. However, without any basis or rationale presented in support of this assertion, it is difficult for the Applicants to understand the basis of these rejections and to provide a proper rebuttal. As best understood, the rejection assumes that because the digital interface 105 of Kobayashi comprises a reception buffer 303 and a transmission buffer 302, then the alleged packet processing controller of Kobayashi may perceivably interact or communicate with the link core 101 of Sato in the manner recited by the pending claims. However, this analysis

completely ignores the fact that the link core 101 of Sato only interfaces with the configuration register 111 in ***both*** transmission ***and*** reception. As such, because the rejection has not provided evidence in supporting the argument that the link core 101 of Sato may otherwise interface with the digital interface 105 of Kobayashi in ***both*** transmission ***and*** reception, it is respectfully submitted that the proposed combination is based solely on improper hindsight reasoning, whereby the pending rejection has selected bits and pieces of the claimed invention from plural references and used only Applicants' specification as a guide to reconstruct the claimed invention. Therefore, the proposed combination fails to establish *prima facie* obviousness of the pending claims.

Even assuming *arguendo* that the Examiner's proposed combination is proper, claim 2 recites "a packet processing control timer for clocking how much time has passed since the packet was ***received*** by the link core circuit and for generating a signal when the time passed reaches a predetermined amount of time." In direct contrast, the clocking circuit 305 of Kobayashi is ***specifically*** provided for timing the period beginning when a packet is sent by the control unit 107 of a source and a response to the packet is received from a destination (e.g., from the TV 101) (see, col. 4, [101]-[104] and col. 6, [0142]-[0146]). In other words, the clock circuit 305 functions to measure how much time has elapsed since the packet has been ***transmitted***, rather than ***received***, by the digital interface 105 of the source, rather than by the alleged link core. Also, in an event it is asserted that the time stamp of Sato is interpreted as the claimed packet processing control timer, it is noted that Sato specifically discloses adding a time stamp to the source packet header so as to suppress the time jitter at the time of transmission and to determine the data output time at the reception side (see, col. 6, lines 33-36). As such, Sato also does not cure the defect of Kobayashi, because the time stamp of Sato does not appear to clock the link core 101 in the

manner required by the pending claims. At best, Kobayashi and Sato have arguably shown a timer circuit, a control circuit and a link core without demonstrating how the packet received at the link core is timed, let alone to generate a signal, stop or restart the processing of the received packet in response thereto.

In contrast, as described throughout the admitted prior art section of Applicants' specification, if the data of the received packet cannot be stored successfully in the segment buffer region at the consumer node within a predetermined amount of time as defined by the IEEE 1394 standard, the consumer node cannot return a response packet in response to the request packet issued by the producer node. Accordingly, a time-out is produced at the producer node. Specifically, Applicants have discovered that because the conventional processor does not define how the packet processing should continue at the producer node during such a time-out, a new packet processing transaction is often started while the current packet processing transaction is still incomplete, rendering multiple transactions and resulting in slow and inefficient packet processing at the producer node. Accordingly, by providing a control timer for clocking the time elapsed since a packet has been received, the processor of the present invention does not accept the next request packet until the current transaction is over, such that the consumer node and the producer node can perform the necessary time management to determine when the processing of the received packets should be restarted, carried out or stopped. As a result, a time-out at the transmitting end is advantageously prevented and the packet transaction processing/sequence is greatly simplified.

In this regard, Kobayashi and Sato, at best, are merely cumulative to the admitted prior art described at pages 1-8 of Applicants' specification in that Kobayashi and Sato are also subject to the same drawbacks as those of the admitted prior art resulting from a lack of a timer circuit for clocking the time elapsed since a packet has been received, identified by the instant

inventors at pages 9-10 of Applicants' specification . Only Applicants have recognized and considered the problems associated with the time-out at the producer and/or consumer node, and provided the means by which to overcome such problems. For all of the foregoing reasons, it is respectfully submitted that Kobayashi and Sato, alone or in combination, do not disclose or suggest the claim elements recited by claim 2.

With respect to claim 8, as discussed above, because the rejection has not provided evidence in supporting the argument that the link core circuit 101 of Sato may interface with the digital interface 105 of Kobayashi in ***both*** transmission ***and*** reception it is respectfully submitted that, the pending rejection to claim 8 is improper.

Nonetheless, in an effort to advance prosecution and to assist the Examiner in understanding the distinctions between the present invention and the cited prior art, claim 8 has been amended to recite in-part "a packet processing control timer for clocking how much time has passed ... and for generating a signal when the packet to be transmitted is not sent out after the time passed reaches a predetermined amount of time, wherein the controller stops generating the packet to be transmitted ... and restarts generating the packet to be transmitted when another transaction processing performed by the CPU ends."

Specifically, in accordance with one exemplary embodiment of the present invention, data is supplied from the memory 40 to the controller 20 of the processor 3 to generate a BWRQ packet at the producer node (e.g., the DVC 300), such that the controller 20 produces a BWRQ packet to be transmitted and outputs a control signal CT2b to the timer 22 for starting the clock. If the BWRQ packet is not transmitted after a preset time has elapsed since the BWRQ packet is generated, the timer 22 detects a time-out and informs the CPU accordingly. Additionally, the timer 22 outputs a control signal CT2a to the controller 20, such that the controller 20 stops

generating BWRQ packets. Once the preset time reaches a predetermined threshold, the CPU performs heartbeat processing, causing the controller 20 to restart generating BWRQ packets (see, e.g., page 34, lines 6-23 of the specification).

In contrast, Kobayashi and Sato, alone or in combination, are silent with regard to any preset time, let alone suggest generating a signal when a packet to be transmitted is ***not*** sent out if such a preset time is reached. Additionally, the alleged processing control timer (clocking circuit 305) of Kobayashi appears to be applicable only to the receiving side for receiving the packets via the ports 1 and 2 (see, Fig. 3). As such, the alleged processing control timer of Kobayashi does not apply to the transmission buffer 302of the transmitting side, let alone measure the period between which the packet is generated and transmitted therein. Also, Kobayashi is silent with regard to any transaction processing performed by a CPU, let alone disclose ***stopping*** or ***restarting*** the packet generation when such a CPU transaction has ***ended***. Sato is silent with regard to utilizing a controller, let alone perform the specific functions as recited by claim 8, and therefore, does not cure these defects of Kobayashi.

It should be recognized that the fact that the prior art could be modified so as to result in the combination defined by the claims at bar would not have made the modification obvious unless the prior art suggests the desirability of the modification. *In re Deminski, 796 F.2d 436, 230 USPQ 313 (Fed. Cir. 1986).*

Moreover, recognizing after the fact that such a modification would provide an improvement or advantage, without suggestion thereof by the prior art, rather than dictating a conclusion of obviousness, is an indication of improper application of hindsight considerations. Simplicity and hindsight are not proper criteria for resolving obviousness. *In re Warner, 379 F.2d 1011, 154 USPQ 173 (CCPA 1967).*

It is only Applicants' disclosure that discloses the claimed processor. Neither Kobayashi nor Sato disclose or suggest such a processor. Thus, the only motivation of record for the proposed modification of the method for transmitting packets of Kobayashi to arrive at the claimed invention is found in Applicants' disclosure which, of course, may not properly be relied upon to support the ultimate legal conclusion of obviousness under 35 U.S.C. § 103. *Panduit Corp. v. Dennison Mfg. Co., 810 F.2d 1561, 2271 USPQ2d 1593 (Fed. Cir. 1987).*

Thus, as each and every limitation must be either disclosed or suggested by the cited prior art in order to establish a *prima facie* case of obviousness (see, **M.P.E.P. § 2143.03**), and Kobayashi and Sato, alone or in combination, fail to do so, it is respectfully submitted that amended claim 8 is patentable over the cited prior art.

With respect to new claim 13, this claim incorporates all elements included in canceled claim 1 and original claim 3. Specifically, this claim recites in-part "while processing the received packet, the controller prohibits the link core circuit from receiving another packet delivered externally through the bus." Importantly, by prohibiting the link core circuit from receiving another packet, the processor of the present invention does not accept the next request packet until the current transaction is over. However, as is apparent from the foregoing discussion, the cited prior art is completely silent with regard to any need for awaiting the completion of the current packet transaction, let alone implement a processor for refusing to accept any further packet during such transaction. For at least this reason, it is respectfully submitted that new claim 13 is also patentably distinct over the cited prior art.

It is noted that the pending rejection references various portions of Kobayashi and Sato as allegedly disclosing the claimed features, but does not identify ***precisely which elements*** (neither by reference numerals nor by written explanation) of Kobayashi and Sato are being read on the respective claimed features. It appears that the Examiner has copied and pasted the cited paragraphs directly from the cited references without providing explanation with regard to how the prior art method for transmitting packets of Kobayashi or the signal processing circuit of Sato carries the same functionalities as those recited by the rejected claims. If the Examiner maintains the pending rejection, it is respectfully requested that the Examiner identify which specific element or function of Kobayashi or Sato reads on ***each*** and ***every*** limitation recited in the pending claims rather than merely pointing Applicants to wide-ranging disclosures (e.g., page 4, paragraph [0094] of Kobayashi and col. 4, line 35+ of Sato) of Kobayashi and Sato so as afford the Applicants an opportunity to rebut and/or address the specific elements or functions identified as reading on the pending claims.

III. All Dependent Claims Are Allowable Because The Independent Claims From Which They Depend Are Allowable

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co., 819 F.2d at 1100, 1108 (Fed. Cir. 1987).* Accordingly, as independent claims 2, 8 and 13 are patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also in condition for allowance.

IV. Conclusion

Accordingly, it is urged that the application is in condition for allowance, an indication of which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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Date: March 7, 2005